

This is the web version of a paper that appeared in *Analog Integrated Circuits and Signal Processing*, Vol. 42, pp. 161-178, 2005. The original publication is available at [www.springerlink.com](http://www.springerlink.com):

<http://www.springerlink.com/openurl.asp?genre=article&eissn=1573-1979&volume=42&issue=2&spage=161>

## **A Methodology for Long Time Constant Log-Domain Filters in CMOS**

Patrick Shoemaker

**Abstract** — A simple methodology for implementation of low-order, current-mode, log-domain filters in CMOS technology is presented. The key transistors in the circuit are operated in weak inversion and in contrast with previous approaches may pass into the triode regime. The concept is particularly suited to implementation in silicon-on-insulator technology, because dielectric isolation of the transistors eliminates leakage currents, and because influence of the body effect on circuit function is limited. Very long time constants, on the order of 1s or more, are obtainable. A simple elaboration of the basic unit circuit allows the time constant to be controlled by a bias current.

**Keywords** — analog filters, weak inversion, log-domain filters, analog CMOS, silicon-on-insulator.

### I. INTRODUCTION

Active analog filter circuits today find what are probably their most significant applications in the context of anti-aliasing and signal conditioning at the front-end or output of data conversion systems. Many such circuits operate at relatively high frequency, with audio applications perhaps the lowest. However, in contrast with artificial electronic systems, biological signal processing often involves temporal elements with much longer time constants: the general operation of input signal integration by nerve cells may have time constants in the millisecond range, whereas processes associated with adaptation can have characteristic times of hundreds of milliseconds to seconds. For the purposes of emulating neurobiological signal processing it is desirable to implement long time-constant elements in a ‘natural’ fashion, with asynchronous circuits to avoid the propagation of clock noise, and to do so with compact circuits that permit multiple parallel implementation. In biologically-inspired algorithms with parallel and redundant, statistically-based processing, high precision and linearity may in many cases be less important

than in classical data acquisition and signal conditioning. In this paper, we consider an approach to a log-domain filter that may be particularly suitable for such biomimetic applications.

The notion of log-domain filtering was first introduced in 1979 [1], and recently the approach has seen an increase in interest, with parallel development of circuits and applications [2]-[9] and general design methodologies [10]-[12]. Log-domain filters are current-mode circuits that are linear in their inputs and outputs, but in which temporal processing takes place on logarithmically compressed internal voltage variables. The log-domain approach offers several potential advantages: tunability across a very broad range of frequencies; operability over an equally broad range of bias conditions, including low power and low voltage operation; and natural compatibility with the range of nonlinear processing offered by the translinear technique. It relies on primitive devices with an exponential current-voltage relationship, and most reported implementations of log-domain filters have been with monolithic bipolar junction transistors. However, because the MOS transistor biased in weak inversion also follows an exponential relationship between drain current and gate-to-source voltage, implementations based on MOSFETs are practical as well. In contrast to the BJT, the MOS transistor has the advantage of a high-impedance control terminal, but many other disadvantageous features, including generally poorer device matching and the presence of the body effect due to substrate bias. These must be addressed by design and/or layout techniques to avoid or reduce negative impact on circuit performance.

In the original conception of the log-domain filter, a basic unit comprising a damped or 'leaky' integrator was presented [1], but in many log-domain filter implementations, the functional unit is a perfect integrator. (Naturally, this unit is an idealization that in real implementation is always subject to some small degree of leakage due to current mismatches and other nonidealities.) This paper presents a concept based on the damped integrator as the fundamental unit. In contrast with typical approaches in which devices are operated in the saturation (MOS) or forward-active (BJT) regimes, this concept allows operation of the key transistors down into the triode regime. It relies on the extremely high gate resistance of the MOS transistor, and on the continuous weak-inversion device characteristics from saturation through triode mode. This last feature, in combination with deep subthreshold operation, permits the implementation of very long time constants, although these may ultimately be limited by junction leakage currents in bulk silicon. Realizations in bulk silicon CMOS and silicon-on-insulator are presented. Due to device mismatches and other physical effects in MOS transistors,

it is anticipated that the method will lend itself most readily to low-order filter topologies and applications in which typical metrics of linear circuit performance, such as precision and low distortion, are not highly critical. Rather, the goal is to provide a circuit that is capable of achieving long time constants in a very compact implementation that is suitable for large-scale, parallel integrated systems.

## II. PRINCIPLE OF OPERATION

For the purpose of developing the principle of operation of the circuits described in this paper, consider first an idealized model of the MOSFET, subject to three simplifying assumptions: the body effect is absent; leakage currents from source/drain regions are negligible; and channel current is independent of drain-to-source voltage when the device is in saturation. (These assumptions will be lifted and the implications of nonidealities in real transistors will be considered in Section IV).

Consider the circuit depicted schematically in Figure 1 below, under these assumptions:

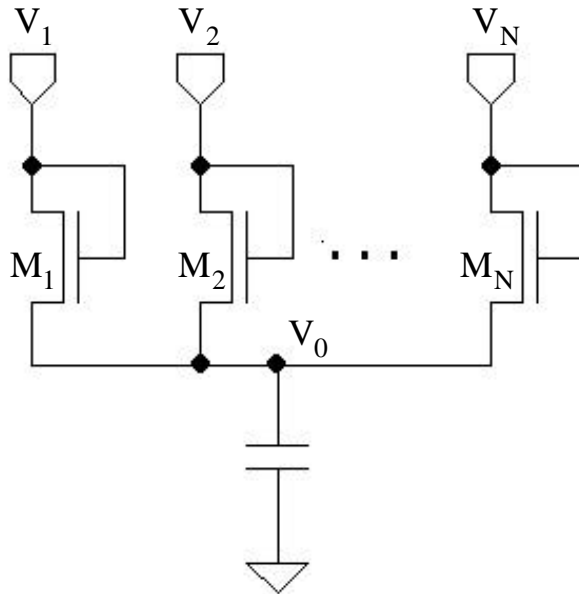


Fig. 1. Basic circuit illustrating the principle of operation of the log domain filter.

If all transistors in Fig. 1 operate in weak inversion, they behave as exponential diodes, and the channel current in any device may be written in the form  $I_i = I_{0i}(\exp[(V_i - V_0)/U_T] - 1)$ ,  $i = 1 \dots N$ . Here  $I_{0i}$  represents the saturation current at zero gate

bias (i.e., the specific current parameter) for the transistor identified by index  $i$ ,  $U_T$  is the thermal voltage, and positive current is taken as flowing into the common drain/source node. Kirchhoff's current equation for that node may be written:

$$C \frac{dV_0}{dt} = \sum_{i=1}^N I_{0i} (\exp[(V_i - V_0)/U_T] - 1) \quad (1)$$

For convenience, define *pseudovoltages*  $\mathbf{y}_i$  according to

$$\mathbf{y}_i \equiv U_T \exp(V_i / U_T), \quad i = 0 \dots N \quad (2)$$

With this definition, Equation (1) can be rewritten

$C(dV_0/dt)\mathbf{y}_0 = CU_T(d\mathbf{y}_0/dt) = \sum_{i=1}^N I_{0i}(\mathbf{y}_i - \mathbf{y}_0)$ . Note that the pseudovoltages as defined are analogous to those used in the analysis of pseudolinear networks based on the linear current division principle for MOSFETs [13] when operated in weak inversion. As in that application, the transistors (which may be regarded as nonlinear resistors) may implicitly operate in the triode regime, and current may flow through their channels in either direction. In addition, the capacitor is connected in a way that enforces a decreasing exponential dependence of the charging current on its plate voltage (characteristic of a log domain filter), resulting in an effective linearization with respect to the dynamic behavior as well. The circuit is thus analogous to an RC circuit of the same topology. In terms of the pseudovoltage  $\mathbf{y}_0$ ,

$$\left( 1 + \frac{CU_T}{\sum_{j=1}^N I_{0j}} \frac{d}{dt} \right) \mathbf{y}_0 = \frac{\sum_{i=1}^N I_{0i} \mathbf{y}_i}{\sum_{j=1}^N I_{0j}}. \quad (3)$$

This explicitly shows the essential features of the analogous linear circuit: voltage division and formation of a real pole with respect to the common node voltage. The pseudovoltages  $\mathbf{y}_i$  play the roles of the voltages and the quantities  $U_T/I_{0i}$  those of the resistances in the circuit. The time constant takes the value

$$\mathbf{t} = \frac{CU_T}{\sum_{j=1}^N I_{0j}}. \quad (4)$$

Because values of the specific current parameter for MOS transistors are typically very small, this circuit can in theory implement poles with very long natural time constants.

Note the isomorphism of the defined pseudovoltages with the drain currents of MOS transistors in weak inversion and in saturation, as functions of gate voltage. When MOS devices

are used at the inputs as compressive elements, and another with its gate tied to the voltage  $V_0$  is used as an expansive output element, then the circuit can be used in practice to implement a weighted summation and/or real pole in the current domain. This is the basis for the filter implementations to be discussed in the following sections.

### III. CURRENT MODE FILTER IMPLEMENTATIONS

In this section, implementation of current-mode filters is considered, under the assumption of idealized MOS transistors as in Section II.

#### A. A Prototype

Application of the principle of operation in Section II may be illustrated by considering the basic single-input prototype circuit depicted in Fig. 2 below:

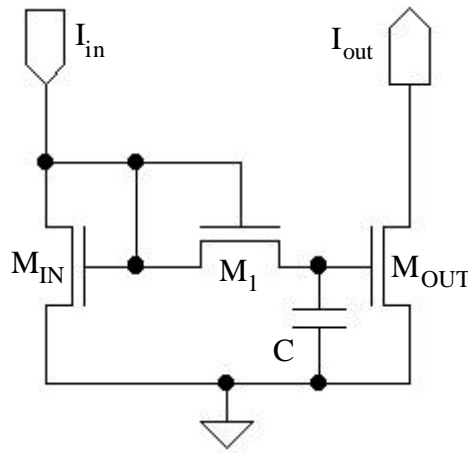


Fig. 2. Prototype for first-order log domain filter with current input and output.

The transistors  $M_{IN}$  and  $M_{OUT}$  in this circuit are presumed to be matched. In addition to the assumptions of Section II, also assume that  $M_{IN}$  and  $M_{OUT}$  remain in saturation, and all gate currents as well as the channel current in  $M_1$  are negligible compared to  $I_{in}$ . Under these conditions,  $M_{IN}$  acts as a nonlinear load and also provides a low impedance for charging the  $M_1 - C$  circuit. The input – output relation for the circuit is then simply

$$\left(1 + \frac{CU_T}{I_{01}} \frac{d}{dt}\right) I_{out} = I_{in}, \quad (5)$$

where  $I_{01}$  is the saturation current at zero gate bias for  $M_1$ ,  $C$  is the capacitance value of the capacitor  $C$ , and the time constant takes the value  $t = CU_T / I_{01}$ . The circuit is a damped integrator in the current domain, suitable for class A operation.

As a practical matter, if the aspect ratios of  $M_{IN}$  and  $M_1$  are comparable, the requirement that  $M_{IN}$  remain in saturation is sufficient to insure that  $I_{in}$  dominates the channel current in  $M_1$ : it is easily shown that the drain current of  $M_{IN}$  differs from the channel current of  $M_1$  by a factor of at least  $I_{0M} I_{in} / I_{01}^2$ , where  $I_{0M}$  is the specific current for the input and output devices; when  $M_{IN}$  is in saturation,  $I_{in}$  is necessarily much greater than  $I_{0M}$  and so this factor is much larger than one.

A simple modification to this prototype is obtained by buffering the gate voltage of  $M_{IN}$ , for example in a common-drain common-source feedback configuration as in Fig. 3 below. In principle, this buffer extends the operating range of the filter at the low end by decoupling  $M_1$  and the gate of  $M_{IN}$  from the input node, and it maintains  $M_{IN}$  in saturation for very low gate voltages (although in practice the current source may fall out of compliance when implemented with a real transistor).

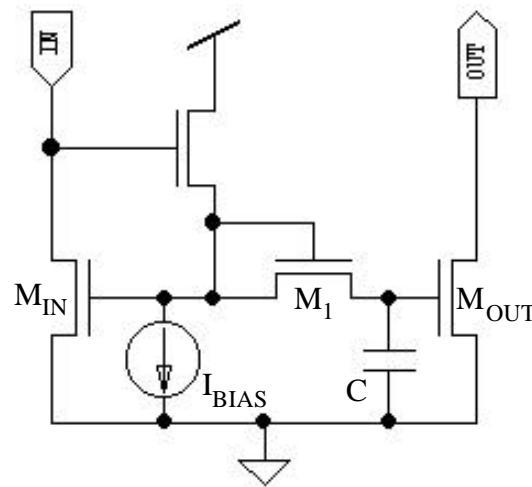


Fig. 3. Voltage buffering at the input of the basic lowpass filter circuit.

The bandwidth of the follower circuit in Fig. 3 must exceed that of the filter itself, in order to assure first-order, linear lowpass behavior above the corner frequency.

The time constant associated with the basic circuit is determined by the choice of aspect ratio of transistor  $M_1$  and the capacitance of  $C$ , but it is fixed for any particular physical design, and in most CMOS processes would be restricted to relatively large values. Additionally, in a practical

implementation it is ultimately dependent upon (possibly poorly controlled) process characteristics as well as temperature. To make the circuit practically useful, a means of electrical control of the tuning is desirable. This can be achieved by level-shifting the gate voltage of transistor  $M_1$  relative to that of the input device by a controlled amount, as with the source-follower circuits shown in Fig. 4 below.

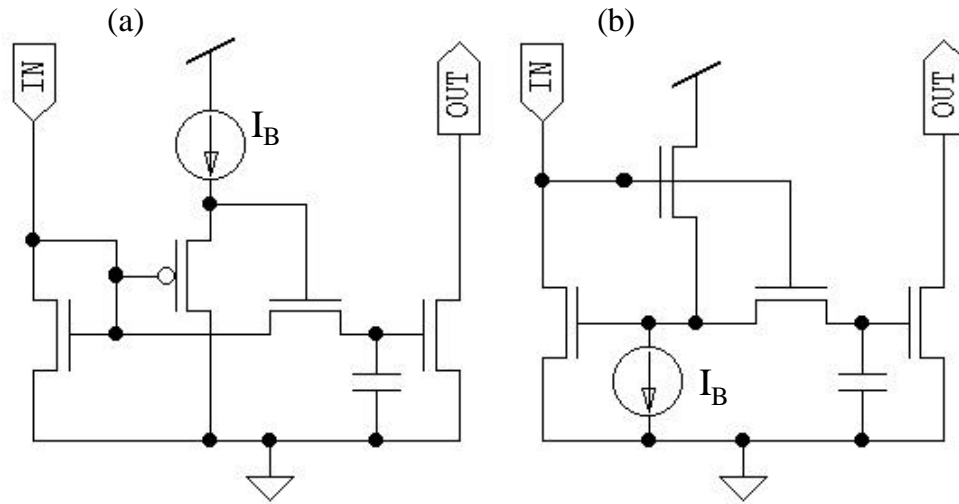


Fig. 4. First-order lowpass filters with level-shifting followers to modify time constant. In (a) the gate voltage of the nonlinear resistor device is shifted by a follower transistor of the opposite type. In (b), it is shifted by connecting it to the gate of a buffer otherwise configured as in Fig. 3.

The level-shifts introduced by the circuits in Fig. 4 are restricted by the bandwidth requirements of the circuit (which will be further discussed in Section IV). The circuit of Fig. 4b provides the advantage of input voltage buffering in addition to level shifting. The time constant  $\tau$  of the basic circuit in Fig. 2 is multiplied by a factor  $\exp(-V_{LS}/U_T)$  in the modifications of Fig. 4, where  $V_{LS}$  is the level shift introduced by the follower.

### B. Further Filter Topologies

With the use of active circuits including current mirrors for signal duplication and inversion, and when necessary voltage buffers, a range of filter topologies based on the series R – grounded C unit cell may in theory be synthesized. For purposes of illustration, some basic examples are given here.

Implementation of a first-order highpass unit cell complementary to the lowpass prototype is particularly simple, requiring only summation of a copy of the input current with the output of



source stage, which is limited on the low side by the negative supply, then it performs a half-wave rectification and low-pass filtering of the input signal. The drain current of the input device does not identically represent the positive phase of the input signal, as the input voltage cannot be driven all the way to ground, but will be a close approximation. This may be of use for gain control or other adaptive circuitry in applications when an estimate of signal magnitude needs to be made using a very simple circuit.

If the input and output transistors of the basic prototype circuit in Fig. 2 are driven into moderate or strong inversion, the pseudolinearity of the circuit is lost, but an interesting behavior ensues: a marked asymmetry prevails between charging (input current increasing) and discharging (input current decreasing) behavior. When the input and output devices are in strong inversion, while the nonlinear resistor  $M_1$  remains in weak inversion, the input-output relationship may be written (using the Heaviside notation)

$$I_{\text{out}} = \left( \frac{KU_T^2}{2} \right) \ln^2 \left[ \frac{1}{(1 + \tau \, d/dt)} \exp \left( \sqrt{\frac{2I_{\text{in}}}{KU_T^2}} \right) \right], \quad (6)$$

where  $K = \mathbf{n}C_{ox}W/L$  is the transfer constant typically used to characterize MOSFETs in strong inversion, and where the time constant  $\mathbf{t} = CU_T/I_{01}$  is identical to that for the basic circuit. Integration of this equation for the case of step inputs yields results such as those in Fig. 6:

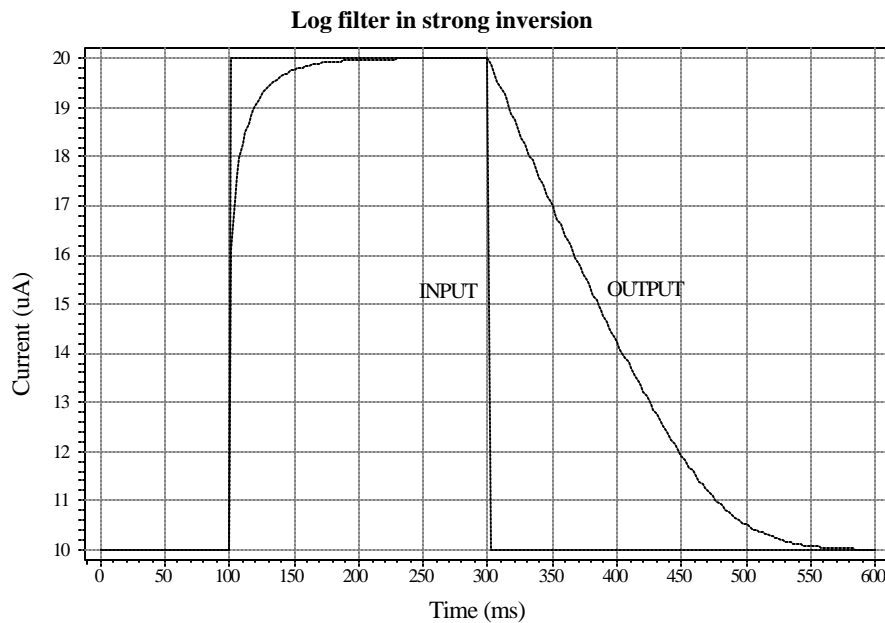


Fig. 6. Simulated response of the first-order lowpass filter prototype when operated in strong inversion. Parameters in Eqn. (6) are:  $t = 25\text{ms}$ ;  $K = 100\mu\text{A}/\text{V}^2$ ;  $U_T = 25\text{mV}$ .

This behavior may be useful for nonlinear gain control applications, for example as a peak detector, or to model temporal phenomena with fast onset and slow decay characteristics in analog circuitry. Similar behavior can be obtained with variants of the filter circuit in which a sub-exponential current-voltage relationship is imposed on the input and output devices by design, for example by the use of cascode transistors that force them to operate in the triode regime.

#### IV. DEVICE NONIDEALITIES AND PRACTICAL ISSUES

The log-domain circuit concept described in Sections II and III was developed under the simplifying assumptions that the MOSFET body effect, the leakage current from the integrating node, and the dependence of transistor channel current on drain voltage in saturation were all negligible. This last condition can be addressed by the use of long-channel transistors and/or cascode devices to increase output resistance. However, leakage current and the body effect are unavoidable in bulk silicon and would be expected to affect operation of the circuit.

For this reason, silicon-on-insulator processes are regarded as a promising medium for implementation: dielectric isolation of individual transistors eliminates junction leakage, and although body effect is present in subthreshold operation, its influence on the temporal characteristics is limited because large potential differences between the source and undepleted body are not generally possible if the body is not tied to an external potential. However, the characteristics of SOI devices can be expected to introduce their own performance issues and limitations.

The implications of nonideal device characteristics, both in general and particular to bulk CMOS and silicon-on insulator processes, are considered below. In a number of cases, the distortion introduced by these nonidealities in the basic lowpass filter circuit is discussed. Distortion is evaluated at the corner frequency of the circuit, where it is relatively high, and for relatively large signals (modulation factor 0.5), but it is worth noting that distortion in the passband is expected to be quite low, as the circuit acts essentially as a current mirror for such frequencies.

In addition to the effects of circuit nonidealities, issues related to practical implementation of specific filter circuits and modifications detailed in Section III are also discussed in this section.

### A. Implementation in Bulk Silicon

In the basic damped-integrator circuit as implemented in bulk silicon, leakage current from the integrating node will typically be present in the form of reverse junction current in a pn junction. Under practical operating conditions the junction will be subject to a limited range of reverse bias voltages and will draw a near-constant leakage current  $I_{0j}$ . A constant current sunk from the integrating node of a log-domain integrator has the effect of damping the integrator; i.e., it acts as a parasitic pseudo-resistor (of resistance  $U_T/I_{0j}$ ) connecting the integrating node to ground. The pseudolinearity of the circuit is not affected, but as in the linear case the parasitic resistance imposes an upper limit on the magnitude of the time constant that can be attained, and affects the voltage division when the resistances of the transistors in the circuit are not significantly smaller than  $U_T/I_{0j}$ .

In contrast with the influence of junction leakage, the body effect does affect the external linearity of the circuit. For the transistors depicted in Fig. 1, assuming that the common body of all devices is at ground potential, the channel currents become  $I_i = I_{0i} \exp[V_i / (\mathbf{h}U_T)] [\exp(-V_0 / U_T) - \exp(-V_i / U_T)]$ , where  $\mathbf{h}$  is the body factor. The body factor is only a weak function of gate-to-substrate voltage, and so if the applied voltages remain similar in magnitude, it can be assumed to be nearly equal for all devices. (Conversely, if the input voltages differ significantly, those that are smallest make a negligible contribution to the voltage associated with the circuit output). With a modified definition of the pseudovoltages,

$$\hat{y}_i \equiv U_T \exp(V_i / (\mathbf{h}U_T)), \quad i = 0 \dots N, \quad (7)$$

and noting that the input and output currents in a log-domain filter are proportional to these  $\hat{y}_i$ , it can be shown that a governing equation analogous to (3) may be written:

$$\left( \frac{\hat{y}_0}{U_T} \right)^{(h-1)} \left( \frac{\mathbf{h}CU_T}{\sum_{j=1}^N I_{0j}} \right) \frac{d}{dt} \hat{y}_0 + \left( \frac{\sum_{i=1}^N I_{0i} (\hat{y}_0 / \hat{y}_i)^{(h-1)}}{\sum_{j=1}^N I_{0j}} \right) \hat{y}_0 = \frac{\sum_{i=1}^N I_{0i} \hat{y}_i}{\sum_{j=1}^N I_{0j}}. \quad (8)$$

With the equation in this form, the influence of the body effect can be regarded in terms of several factors. The time constant of the idealized circuit,  $CU_T / \sum_{j=1}^N I_{0j}$ , is multiplied by  $\mathbf{h}$ , which (being only weakly dependent on the filter state) can be interpreted as arising from reduction of the small-signal conductance of the nonlinear resistor due to reduction of the log slope of its I/V relation, and an additional factor  $(\hat{y}_0 / U_T)^{h-1}$ , which (being strongly state-

dependent) may be regarded as reflecting a large-signal shift in the conductance due to the prevailing source-to-body bias. This last factor may vary by orders of magnitude depending upon the output pseudovoltage. However,  $h$  typically takes values well under 2.0, so the exponent in the factor is fractional, and it may be quite practical to limit variations of  $\hat{y}_0$  about its mean (e.g., by choice of dc bias at the inputs) such that the net time constant varies little. Such limitations also render the factor multiplying  $\hat{y}_0$  close to unity, so that the principal result of the body effect for small signals is an increase in the time constant with increasing mean current levels.

In particular, when a small-signal analysis is performed for the prototype circuit of Section III-A, the governing equation is found to take the form

$$\left[ 1 + \left( \frac{I_B}{I_{OM}} \right)^{(h-1)} \left( \frac{hCU_T}{I_{OI}} \right) \frac{d}{dt} \right] i_{out} = i_{in} , \quad (9)$$

where the input comprises a small signal  $i_{in}$  superposed on a dc bias  $I_B$ , and  $i_{out}$  is the small-signal output current. As in Section III A,  $I_{OM}$  represents the specific current parameter of the input and output devices, and  $I_{OI}$  that of the nonlinear resistor. The time constant is increased relative to the value for the ideal transistor circuit, by a factor proportional to the body factor and to the bias current to the power  $(h-1)$ . Implicit in the derivation of Equation (9) is the assumption that the body factors of the input/output devices are the same as that of the nonlinear resistor; because their gate-to-substrate voltages are essentially the same, this assumption is justified.

Even though multiple nonlinearities are present in the full nonlinear equation (8), their relative weakness under many practical circumstances means that relatively large periodic signals may be passed with relatively modest distortion. When the complete equations for the prototype circuit of Section III A are integrated in simulations with  $h = 1.4$ , and with sinusoidal input signal of amplitude equal to the half of the mean bias current (modulation factor 0.5), the total harmonic distortion is found to be about 3.8% at the corner frequency, and the mean output current is about 2% smaller than the mean input current. The corner frequency varies as the mean current to the power  $(1-h)$ , as expected.

Thus, a bulk silicon implementation of a basic log domain filter may be practical under particular circumstances and limitations. However, for general signals with nonstationary means, the influence of the body effect (in particular the dependence of the time constant on the mean filter state) presents an obstacle to applications.

### *B. Implementation in Silicon-on-Insulator*

Implementation in a silicon-on-insulator technology that affords dielectric isolation of individual devices eliminates junction leakage from the integrating node of the basic circuit, so that leakage current cannot limit the range of time constants that can be achieved.

The body effect is present in silicon-on-insulator in the sense that a gate-bias-dependent depletion layer is present under the gate of a transistor, with an undepleted ‘body’ region of silicon beneath, during subthreshold operation. Due to the presence of pn junctions between this undepleted region and the source and drain, the potential of the undepleted silicon would be expected to follow that of the source of the transistor under dc and low-frequency conditions. (This expectation may not strictly hold in the presence of significant back interface effects.) The body effect in SOI results in decrease in the log-slope of the drain current as a function of gate voltage to values smaller than  $I/U_T$ , just as in bulk silicon. However, the absence of significant source-to-substrate potential differences means that large bias-related shifts in the time constant of the basic circuit are not present. An analysis based on a simple model of the composite device shows that current in the diode-connected subthreshold MOSFET as a function of applied voltage  $V$  goes approximately as  $[exp(V/(hU_T))-1]$ , where  $h$  is the effective body factor, for  $V$  of magnitude several  $U_T$ . Thus, when serving as the nonlinear resistor in the log-domain filter, it behaves as a near-ideal exponential diode, with only modest deviations from ideality caused by the ‘floating body’.

However, the ‘floating body’ does imply that input and output transistors may have significantly different gate-to-body biases than the nonlinear resistor(s) (whose mean gate-to-body bias is near zero), with resulting differences in their body factors. To examine this effect in the prototype lowpass filter circuit of Section III-A, suppose that the effective body factor is  $h_M$  for the input/output devices, and  $h$  for the nonlinear resistor(s). The pseudovoltages are then related to the input and output currents as

$$\mathbf{y}_1 = U_T (I_{in} / I_{0M})^{h_M/h}; \mathbf{y}_0 = U_T (I_{out} / I_{0M})^{h_M/h}. \quad (10)$$

Assuming that linearity prevails in the relationship between pseudovoltages, then the input-output relationship takes the form (using the Heaviside notation)

$$I_{out} = I_{0M} \left[ \frac{1}{1 + \mathbf{t} \, d/dt} \left( \frac{I_{in}}{I_{0M}} \right)^{h_M/h} \right]^{h/h_M}. \quad (11)$$

Because of the weak dependence of the body factor on bias, the distortion introduced by this nonlinearity is modest. In simulations of the prototype lowpass SOS filter with  $h_M = 1.25$  and  $h = 1.4$ , and sinusoidal input with modulation factor 0.5, the total harmonic distortion is found to be about 0.3% at the corner frequency, and the mean output current is about 0.3% smaller than the mean input current.

It should be noted that channel leakage currents (i.e., effective saturation currents at zero gate bias) in SOI are typically greater than in bulk CMOS, so achievable time constants may be smaller than in bulk. Finally, it should also be noted that the ‘‘kink effect’’ in SOI transistors, reflecting a combination of floating substrate and back interface effects in the presence of hot carriers, has the potential to reduce the drain resistance of input and output transistors and thus affect the accuracy of the circuit.

### C. General Matching of Log Characteristics

In addition to differences in gate-to-body bias, second-order effects related to differences in geometry and bias between the input/output devices and the nonlinear resistor(s), can also result in differences in the log-slope characteristics of the devices (which may be expressed in terms of an ‘effective body factor’). For instance, channel leakages in SOI may be considerably higher than in bulk silicon, reflecting back interface and edge effects on transistor behavior, and it is reasonable to assume that log characteristics under low bias conditions might differ significantly from higher-bias values. Relevant second-order effects may be present in bulk silicon as well as SOI, and contribute additional nonlinearities analogous to those in Equation (11) in the bulk silicon implementation.

### D. Transistor Matching

Of the various transistor characteristics subject to random variations between devices, the built-in surface potential is expected to have the largest impact on the circuits discussed herein.

Device-to-device differences in built-in surface potential are typically expressed in terms of threshold voltage variation for devices operated in strong inversion. In weak inversion, the exponential dependence of channel current on surface potential implies a great sensitivity to transistor-to-transistor variations.

There are two principal effects of variations in built-in surface potential on operation of the prototype filter circuit: when occurring among the nonlinear resistor(s) or level-shifters, they result in variations in the circuit time constant as well as (pseudo)voltage division errors in multiple-input circuits; between input and output devices, they affect scaling of currents at the output relative to those at the input(s). This last problem is common to subthreshold current-mode CMOS circuits, and it can be expected to restrict practical filter circuits to relatively low-order and simple topologies; for example, any circuit requiring summation of current signals, such as the second-order lowpass filter stage of Fig. 5, is particularly susceptible to mismatches in the scaling of those signals.

The standard deviation in threshold voltage for minimum-geometry devices in modern CMOS processes is typically on the same order as the thermal voltage  $U_T$ . Thus, techniques to improve matching, such as large transistor areas and common-centroid layouts, are likely to be necessary to reduce mismatches to smaller values. The simplicity of the basic circuit allows physical layouts to remain compact in spite of such measures.

### *E. Circuits for Electrically Controllable Tuning*

In Section III, source-follower circuits were presented as prototypes for a gate voltage level shifter allowing electrical control of the nonlinear resistor in the basic filter circuit. Even when the follower comprises an ideal MOSFET, operation is constrained by the requirement that the circuit bandwidth exceed that of the filter itself. In the circuits of Fig. 4, follower bandwidth and filter bandwidth depend on the follower bias current in a similar manner, and the only means to independently promote follower bandwidth is by relative sizing of devices in the circuit. This approach clearly has practical limits.

The availability of transistors with widely disparate threshold voltages would provide a useful means for implementing level-shifting followers: devices with large threshold magnitudes (i.e., small specific currents) could be used for nonlinear resistor elements, and those with small thresholds for followers. Such is the case in the silicon-on-sapphire process reported in

Section V, in which low-threshold transistors can be fabricated, affording orders of magnitude difference in inherent specific currents of different devices.

In bulk silicon, follower circuits like those in Fig. 4 will be influenced by the body effect in the follower transistor, which affects the level shift imposed on the gate of the nonlinear resistor device. In a follower of type complementary to the transistors in the circuit, as in Fig. 4a, body effect negatively impacts follower bandwidth, and increases both the dependence of the filter time constant on the mean state and nonlinearity of the response. Thus this circuit is unlikely to be of use in bulk silicon.

Although bandwidth remains an issue, the circumstances are reversed for the like-type follower of Fig. 4b: body effect in the follower transistor tends to counter its effect on the nonlinear resistor device in the filter. In fact, because the body factors for the two devices are essentially the same, the dependence of the time constant on the filter state is eliminated entirely, although pseudolinearity of the circuit remains compromised. If all transistors in Fig. 4b share a common substrate voltage of ground, then

$$I_B = I_{0F} \exp[(V_1 + V_{LS1})/\mathbf{h}U_T] \exp(-V_1/U_T) \quad (12)$$

holds for the follower, where  $V_1$  is the voltage at the drain of the input transistor,  $V_{LS1}$  the gate-to-source voltage of the follower,  $I_{0F}$  is the specific current parameter for the follower,  $I_B$  is the follower bias current, and  $\mathbf{h}$  is its body factor. The current in the nonlinear resistor device may be written

$$I_1 = I_{01} \exp[(V_1 + V_{LS1})/(\mathbf{h}U_T)] [\exp(-V_0/U_T) - \exp(-V_1/U_T)] . \quad (13)$$

Solving Equation (12) for  $\exp[(V_1 + V_{LS1})/\mathbf{h}U_T]$  and substituting into (13) yields

$$I_1 = (I_{01}I_B / I_{0F}) [\exp((V_1 - V_0)/U_T) - 1] . \quad (14)$$

From this result, it follows that an equation analogous to (1) holds, and the governing equation for the filter circuit is linear and first order in the pseudovoltages  $\mathbf{y}_0 = U_T \exp(V_0/U_T)$  and  $\mathbf{y}_1 = U_T \exp(V_1/U_T)$ , where  $V_0$  is the voltage at the gate of the output transistor. The results generalize for a multiple-input circuit yielding an equation analogous to (3) for  $\mathbf{y}_0$ , except with

the  $I_{0i}$  replaced by coefficients of the form  $I_{0i}I_B/I_{0F}$ , which reduces the time constant  $\tau$  by the factor  $I_{0F}/I_B$ .

In this case, however, the input and output currents  $I_{in}$  and  $I_{out}$  are not proportional to the  $y_i$ , but rather to  $\exp(V_i/(\mathbf{h}_M U_T))$  and  $\exp(V_o/(\mathbf{h}_M U_T))$ , respectively, where  $\mathbf{h}_M$  is the body factor for the input and output devices. Thus the input-output relation can be written, using the Heaviside notation:

$$I_{out} = I_{0M} \left[ \frac{1}{1 + \tau \frac{d}{dt}} \left( \frac{I_{in}}{I_{0M}} \right)^{\mathbf{h}_M} \right]^{1/\mathbf{h}_M}. \quad (15)$$

Although the time constant of the circuit is not dependent on mean filter state, its input/output relationship remains nonlinear. Again, this nonlinearity remains relatively mild for moderate signal amplitudes and typical values for  $\mathbf{h}_M$ . When the filter equations are integrated in simulations, with  $\mathbf{h}_M = 1.4$  and sinusoidal input with modulation factor 0.5, the total harmonic distortion is found to be about 4.2% at the corner frequency, and the mean output current is 2.6% larger than the mean input current.

The body effect may also be exploited as a means to promote the bandwidth of circuits with like-type followers. This requires a modification with electrically isolated wells, and because most CMOS processes employ n-wells, the approach is depicted below in the p-channel version:

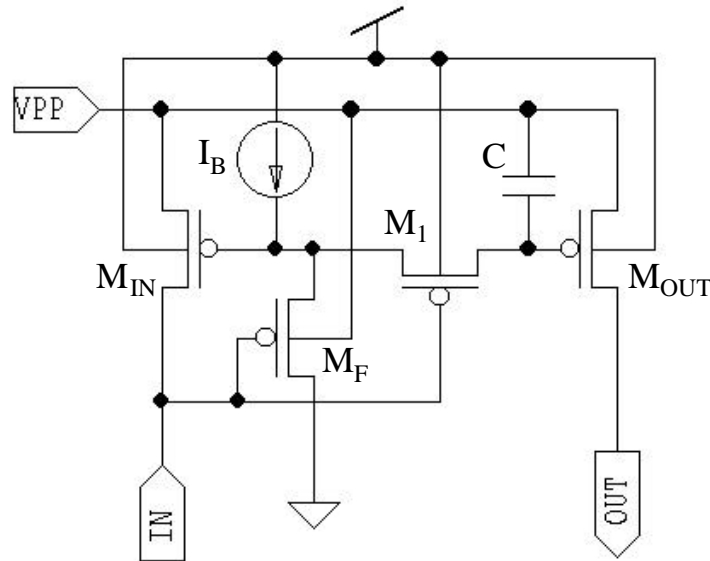


Fig. 7. First-order lowpass filter with level-shifting follower to control time constant. The potential of the terminal labeled VPP is supposed to be lower than  $V_{DD}$  in this circuit. Connection of the follower body to the VPP bias allows promotion of follower bandwidth relative to that of the filter.

This circuit also requires a separate reference (supply) voltage, applied at the VPP port in Fig. 7, which is at a lower potential than the positive supply voltage  $V_{DD}$ . Connecting the follower transistor body to this potential permits it to carry a larger current at a given gate-to-source voltage, than would be the case if the body were maintained at  $V_{DD}$ . This promotes the follower bandwidth relative to that of the filter itself. In addition, the circuit as depicted allows greater headroom for the follower current source to operate. It is readily shown that the circuit input-output relationship follows Equation (15), with the time constant given by  $t = \exp[(1-h)(V_{DD} - V_{PP})/(hU_T)] * (CU_T I_{OF}) / (I_{01} I_B)$ , where  $V_{PP}$  represents the reference potential at node VPP.

In the derivation of this result, it is assumed that the body factors of  $M_F$  and  $M_I$  are not significantly different, in spite of the difference in gate-to-body biases. The implications of differences in these two parameters will not be analyzed here, but simulations were performed in which the body factor for the follower was set to 1.4 and for the input and output devices to 1.3, again with sinusoidal input with modulation factor 0.5. Total harmonic distortion in these results is found to be about 2.7% at the corner frequency, and the mean output current is 1.9% larger than the mean input current.

In spite of the disadvantage of requiring a second supply voltage, this circuit overcomes some of the most serious problems with simpler versions in bulk silicon, and is regarded as the most useful configuration for practical implementation.

#### *F. Noise*

Even though the external input/output relations of the idealized circuit of Section III-A are linear and time-invariant, the internal large-signal nonlinearity means that internally generated circuit noise is subject to nonlinear processing, leading to intermodulation and non-stationary noise at the output [14]. Analysis of output noise has been approached in log-domain filters and closely-related translinear filters by the development of first-order approximations in the device noise currents, and treatment of state dependence and intermodulation of noise with signal currents by considering average noise power at the circuit output [15],[16].

Noise is here analyzed in the idealized circuit, which is depicted below in Fig. 8 with the noise currents associated with each transistor. The fundamental conclusions apply as well to those real versions of the circuit that display time-invariant dynamic behavior (i.e., the SOS circuits and the bulk silicon circuits in Fig. 4b or Fig. 7), although with some quantitative

variations due to the body effect and the minor degree of distortion that is present due to circuit nonidealities.

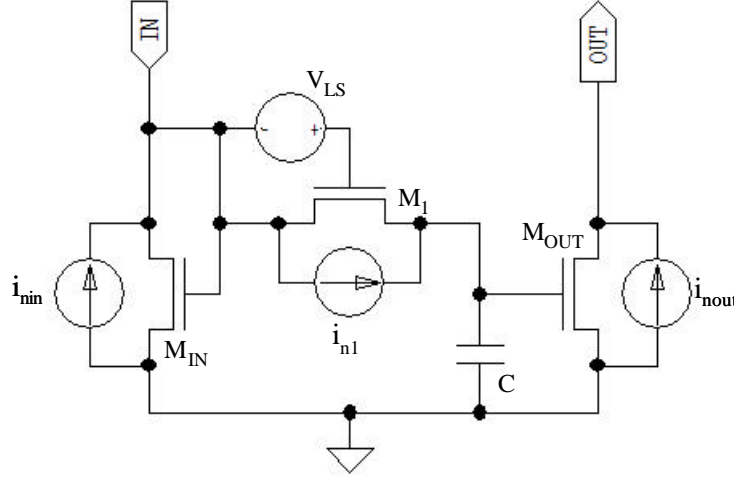


Fig. 8. Idealized basic circuit with schematic depiction of noise currents associated with each transistor.

By inspection of Fig. 8, it can be seen that the noise associated with the output transistor appears directly at the output, while that associated with the input transistor is lowpass-filtered according to the filter transfer function. It can be shown that the relationship between the currents may be written

$$(\tau d/dt + 1)(I_{out} + i_{nout}) = I_{in} + i_{nin} - i_{n1} I_{out} / [I_{01} \exp(V_{LS} / U_T)], \quad (16)$$

where the parameter  $I_{01}$  is as in Section III,  $t = CU_T / [I_{01} \exp(V_{LS} / U_T)]$ , and where terms of higher than first order in the noise currents have been neglected. The final term in (16) represents intermodulation of the noise current associated with  $M_1$  and the output current.

Consider first the white noise portion of the total noise at the output. Sarpeshkar et al. [17] have shown the equivalence of thermal noise to two-sided shot noise, and derived an expression for its power spectral density  $S$  in the MOS transistor biased in weak inversion:

$$S = 2qI_{SAT} (1 + \exp(-V_{DS} / U_T)), \quad (17)$$

where  $q$  is the (unsigned) electronic charge,  $I_{SAT}$  is the saturation current at the given gate-to-source voltage, and  $V_{DS}$  is the drain-to-source voltage. Because the input and output transistors are both in saturation, their contributions to the average white noise power density at the output

are  $2q\overline{I_{in}}/(\mathbf{t}^2\mathbf{w}^2 + 1)$  and  $2q\overline{I_{out}}$ , respectively, where  $\omega$  represents natural frequency and where the overbar indicates average.

The average power spectral density of the intermodulated noise term may be evaluated with the technique adopted by Mulder et al. [15], by means of convolution in the frequency domain of the power spectra of the noise current  $i_{n1}$  and the output current  $I_{out}$ , assuming statistical independence of the two. Using Equation (17) to evaluate the power spectral density of the white-noise portion of  $i_{n1}$  yields the following expression:

$$2qI_{01} \exp\left(\frac{(V_1 + V_{LS})}{U_T}\right) \left[ \exp(-V_0 / U_T) + \exp(-V_1 / U_T) \right] = 2qI_{01} \exp(V_{LS} / U_T) [I_{in} / I_{out} + 1]. \quad (18)$$

Due to its frequency independence, the convolution of (18) with the power spectral density of  $I_{out}$  is simply its product by the average power  $\overline{P_{out}}$  of the output current. Thus, the average power spectral density of the current  $i_{n1}I_{OUT} / [\exp(V_{LS} / U_T)I_{01}]$ , transformed to the filter output, takes the form  $2q(\overline{I_{in} / I_{out}} + 1)\overline{P_{out}} / [I_{01} \exp(V_{LS} / U_T)(\mathbf{t}^2\mathbf{w}^2 + 1)]$ . Substituting for  $I_{01} \exp(V_{LS} / U_T)$  in terms of the time constant  $\tau$  yields  $2\mathbf{t}q(\overline{I_{in} / I_{out}} + 1)\overline{P_{out}} / [CU_T(\mathbf{t}^2\mathbf{w}^2 + 1)]$  for this expression.

Consider now sinusoidal input currents that are superposed with some modulation factor  $m$  ( $0 \leq m \leq 1$ ) on a dc bias current  $I_B$ , and that are well in-band ( $\mathbf{w} \ll 1/\mathbf{t}$ ). In this case,  $\overline{P_{out}} = (1 + m^2/2)(I_B)^2$ ,  $\overline{I_{in} / I_{out}} \cong 1$ , and the contribution of the white noise in device  $M_1$  to the output noise power spectral density is  $4\mathbf{t}q(1 + m^2/2)(I_B)^2 / (CU_T)$ .

It is instructive to compare this quantity to the power spectral contribution of the noise currents in the input and output devices, which totals  $4qI_B$ . When  $\mathbf{t} \gg CU_T / [(1 + m^2/2)I_B]$ , the noise due to the nonlinear resistor device  $M_1$  is dominant. By way of example, for representative values  $C=1\text{pF}$ ,  $I_B=10\text{nA}$ , at maximal modulation  $m=1$ , and at room temperature, the right-hand side of this inequality takes a value of approximately  $1.7\mu\text{s}$ , corresponding to a frequency of over  $90\text{kHz}$ . In many of the anticipated applications of the circuit, the corner frequencies will be set much lower than this, and the white noise due to  $M_1$  will dominate (although of course out-of-band noise will continue to be produced by the output device). In such cases, the total average in-band white noise power is approximately  $4q(1 + m^2/2)(I_B)^2 / (CU_T)$ ,

and the maximal average in-band signal-to-noise-power ratio (at  $m=1$ ) is  $CU_T/(12q)$ . Again by way of example, for  $C=1\text{pF}$  and at room temperature, this ratio is just over 41dB.

At very low frequencies, flicker noise will appear in addition to white noise at the circuit output. The flicker noise power spectral density in an MOS transistor is typically modeled with an expression of the form  $K(I_D)^a/(w^b C_{GOX})$ , where  $K$  is a process-dependent parameter,  $I_D$  is the drain current,  $C_{GOX}$  is the capacitance across the gate oxide of the device, and where the exponents  $a$  and  $b$  are usually around two and unity, respectively. Although the nonlinear resistor device contributes substantially to the total white noise, its flicker noise contribution is generally negligible relative to that of the input and output devices, because its channel currents are typically much lower. The filter circuit behaves like a current mirror with respect to flicker noise, with an average power spectral density at the output of  $2K(I_B)^a/(w^b C_{out})$ , where  $C_{out}$  indicates the gate oxide capacitance of the output (or matched input) transistor. The ‘knee’ of the total average noise spectrum for the circuit occurs when the flicker and thermal noise are comparable, at the frequency  $w = [K(I_B)^{a-1}CU_T/(2qC_{out}[CU_T + tI_B(1 + m^2/2)])]^{1/b}$ . This knee frequency is dependent on the filter corner frequency in addition to being highly process-dependent. By way of example, for the noise models supplied by the foundry for one of the processes (TSMC  $0.35\mu\text{m}$ ) used in the fabricated circuits reported in Section V below, and for corner frequency set to 1Hz ( $\tau = 159\text{ms}$ ),  $C=1\text{pF}$ ,  $I_B=10\text{nA}$ ,  $m=1$ , device size  $W=L=5\mu\text{m}$ , and at room temperature, knee frequencies are calculated to be 0.91mHz for an NMOS circuit and 9.8mHz for PMOS.

Finally, because the level shift  $V_{LS}$  depicted in Fig. 8 is implemented in practice with a source-follower circuit, the noise current in that follower also contributes to the total average noise power spectral density at the output. It can be shown, however, that this contribution is negligible except near the corner frequency, and has essentially no impact on the conclusions reached in this section.

## V. EXPERIMENTAL RESULTS

### A. Circuits Implemented

Single-input, first-order lowpass filter circuits have been fabricated in a thin-film  $0.5\mu\text{m}$  SOS CMOS process (Peregrine Semiconductor), and an  $0.35\mu\text{m}$  bulk CMOS process (TSMC), both

accessed via the MOSIS prototyping service. The configurations implemented are described below for each process.

1) SOS CMOS: PMOS and NMOS versions of the basic prototype as in Fig. 2; PMOS version with electrical control of the time constant using opposite-type follower as in Fig. 4a.

The input and output transistors are configured in common-centroid quads. The nonlinear resistor is implemented with edged and edgeless devices in different test circuits, in order to evaluate possible edge leakage. These devices use the ‘regular’ channel implants available in the process, with measured threshold voltages on the order of 800mV for the n-channel transistors and on the order of -850mV for the p-channel transistors. Effective body factor  $\eta$  is on the order of 1.6 for NMOS and 1.2 for PMOS. The capacitors in all circuits are depletion MOS devices (i.e., bottom plate doping of the same type as the ohmic contact or source region, which matches that of the input/output and nonlinear resistor devices), using the ‘regular’ implants. With their bottom plates connected to the respective power supply voltages, these devices operate in accumulation. In the PMOS version with electrical time constant control, the n-channel follower transistor is fabricated using a ‘low’ channel implant, with measured threshold voltages on the order of 300mV.

2) Bulk CMOS 0.35 $\mu$ m: PMOS version with input buffering and electrical control of time constant, using follower in isolated well and second positive supply voltage, as in Fig. 7.

Input and output transistors are configured as inside matched pairs. Measured PMOS thresholds are on the order of -750mV, and the body factor  $\eta$  at zero source-to-body bias is on the order of 1.35. The capacitor is implemented as an MOS structure in the VPP well, and remains in weak inversion for the test conditions described below.

### *B. Test Configuration and Procedures*

The circuits were all tested with relatively large-signal inputs, in configurations similar to that depicted schematically in Fig. 9 below. In the bulk CMOS circuit, the VPP terminal was biased at 0.5V below VDD. Transconductance and transresistance amplifiers were used to interface to the devices under test, to allow for voltage inputs from and outputs to off-board equipment. These interface amplifiers were implemented with low-noise, low-offset operational amplifiers (TL072C) and metal-film 1% resistors of 2M $\Omega$  for the SOS circuits and 10M $\Omega$  for the bulk CMOS circuit. A function generator (HP 33120A) supplied dynamic inputs to the test circuit. The circuit board carrying the chip and I/O circuitry was enclosed in a Faraday cage during

testing. Output was routed to either a digitizing oscilloscope or a spectrum analyzer (HP3585A) for measurements.

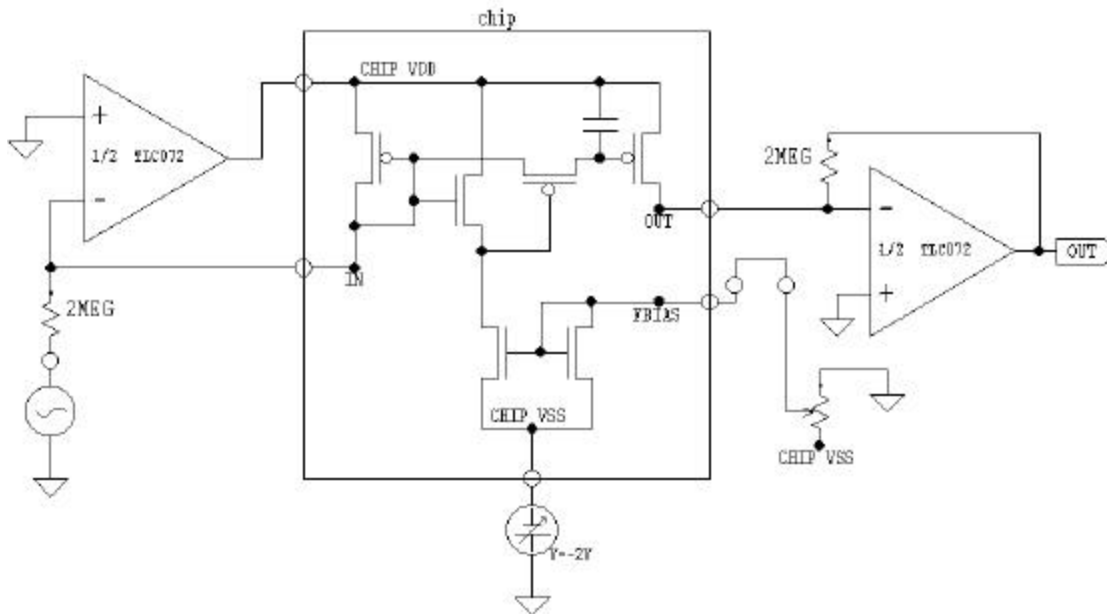


Fig. 9. Example test configuration for filter circuits. The setup for the SOS PMOS lowpass filter with electrical time constant control is depicted. CHIP VSS rather than CHIP VDD is driven for the NMOS circuits, and the potentiometer for biasing the follower is not needed for the basic circuits. In the bulk CMOS circuit, input current is supplied to the PMOS circuit via an NMOS current mirror, so that CHIP VSS is driven in that case as well.

During tests of the circuits in the pseudolinear regime, external inputs consisted of sine or square waves with peak-to-peak amplitudes of 100mV and offsets of  $\pm 100\text{mV}$  (depending on the polarity of the device under test), so that applied input currents varied between 25nA and 75nA for the SOS circuits, and 5nA to 15nA for the bulk CMOS circuits. Lower current levels were used in the bulk circuit in an effort to maintain its MOS capacitor well in weak inversion and thus in a relatively linear regime. For selected tests on the bulk circuit, the mean input current was varied by simultaneously rescaling the amplitude and offset of the input, in order to demonstrate the independence of time constant from filter state. Responses to sine and square wave inputs at various frequencies were observed and recorded with the oscilloscope, for circuits of each type on several different die. Frequency response was evaluated by graphical analysis of the magnitude and phase of the response to sinusoidal input. Control of the time constant in the circuits with level-shifting followers was evaluated over a range of bias currents. Finally, harmonic distortion was analyzed in these circuits. Using sinusoidal input with modulation factor 0.5, the  $-3\text{dB}$  corner frequency and the excitation frequency were set to the same value, and the

harmonic distortion in the output was measured with the spectrum analyzer for three different die. Harmonic distortion was also measured for sinusoidal signals well in the passband.

Operation with input currents in the moderate to strong inversion range was also evaluated in one of the SOS circuits. The response to a square wave input with currents ranging from  $0.5\mu\text{A}$  to  $1.5\mu\text{A}$  was recorded.

### *C. Test Results*

Test results for the circuits described in Section V-A are detailed below in the order in which they were presented in that section.

#### 1) SOS CMOS:

The three filter circuit configurations fabricated in SOS were all found to be operational under the applied test conditions. Behavior of all circuits in response to sinusoidal inputs is consistent with a single pole. For the PMOS and NMOS basic prototype circuits, time constants were calculated from  $-3\text{dB}$  frequencies on samples of five circuits on five different die. These time constants range from 350ms to over 1.2s for the PMOS circuits, and 165ms to 300ms for the NMOS. These values, which reflect the intrinsic properties of the nonlinear resistor device, are considerably smaller than would be predicted from extrapolated specific current parameters based on the drain current / gate voltage relationship at current levels of 1nA and greater. This presumably reflects larger-than-expected channel leakage currents in the nonlinear resistor devices under very low bias conditions. However, little of this is apparently due to edge leakage, since circuits using edged devices displayed measureable but minor reduction in time constants when compared to circuits using edgeless devices of the same aspect ratio.

The PMOS circuit with level-shifting follower was found to allow electrical control of the corner frequency over a range of about five decades, from a decade below the corner frequency of the basic circuit, up to several kHz. This reflects operation with bias currents from a few pA to several hundred nA. A Bode plot generated with data taken from this circuit is shown below in Fig. 10.

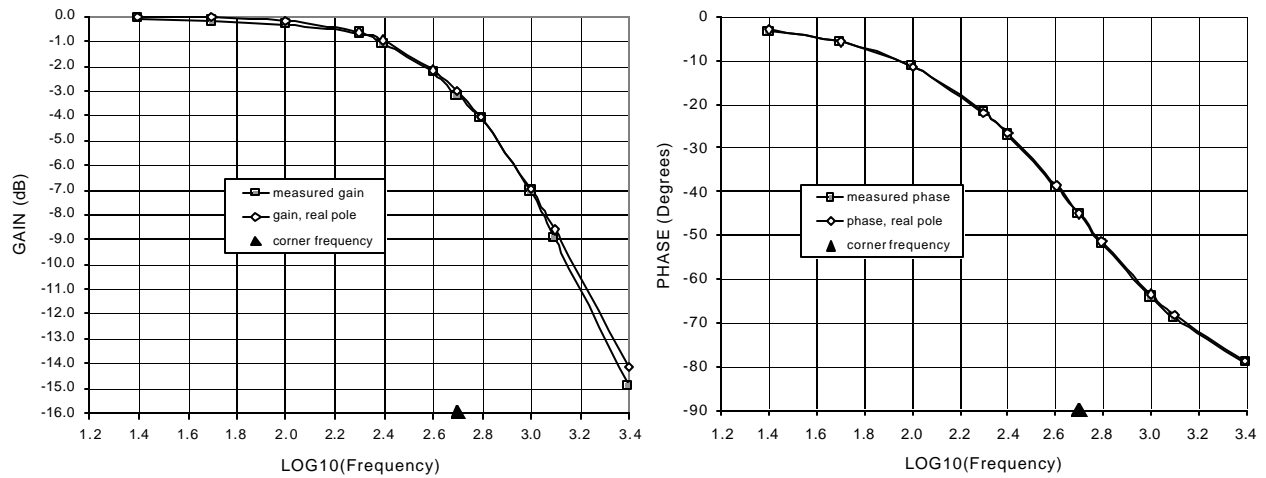


Fig. 10. Bode plots illustrating the frequency response of a SOS PMOS filter circuit with adjustable time constant set to  $320\mu\text{s}$  (corner frequency 500Hz).

Total harmonic distortion with the corner and input frequencies set to 500Hz averages 3.1% in a sample of three die. In the passband, distortion as expected is much lower (values on the order of 0.15% were measured). Distortion measurements on the basic circuits were not practical due to bandwidth limitations.

Operation of this circuit with the input and output devices in the moderate to strong inversion regimes yields strongly asymmetric charge/discharge responses in conformance with the simulated results on Section III-C. An example recording is depicted in Fig. 11.

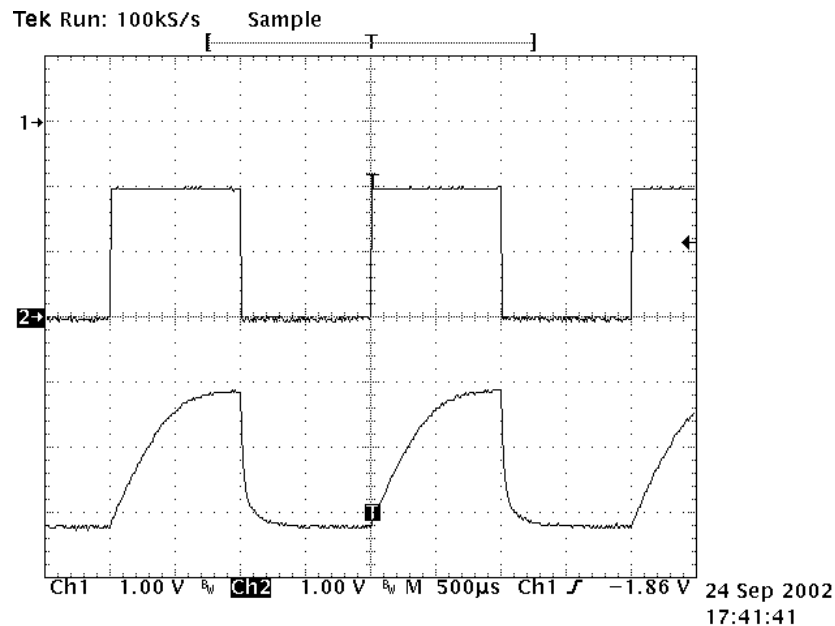


Fig. 11. Dynamic response of PMOS filter circuit with input and output devices in moderate to strong inversion. Input is the top trace (channel 1) and output the bottom trace (channel 2).

## 2) Bulk CMOS 0.35 $\mu\text{m}$ :

The bulk CMOS circuit was found to be operational under the applied test conditions, with behavior consistent with a single pole. A Bode gain plot illustrating tunability of the circuit is shown below in Fig. 12. With VPP biased 0.5V below VDD, corner frequencies below 1Hz and over 20kHz can be obtained. Below 1Hz, the effect of leakage current from the integrating node begins to limit performance (gain in the passband when the corner frequency is 0.5Hz is about 0.90). Above 1kHz, the measurement technique is compromised by capacitive coupling through the substrate (which is driven by the input transconductance amplifier), resulting in feedthrough of the input voltage to the output. However, the follower bias currents required to establish the corner frequencies in Fig. 12 results suggest that it should be practical to tune the circuit to at least several hundred kHz while maintaining the follower transistor in weak inversion.

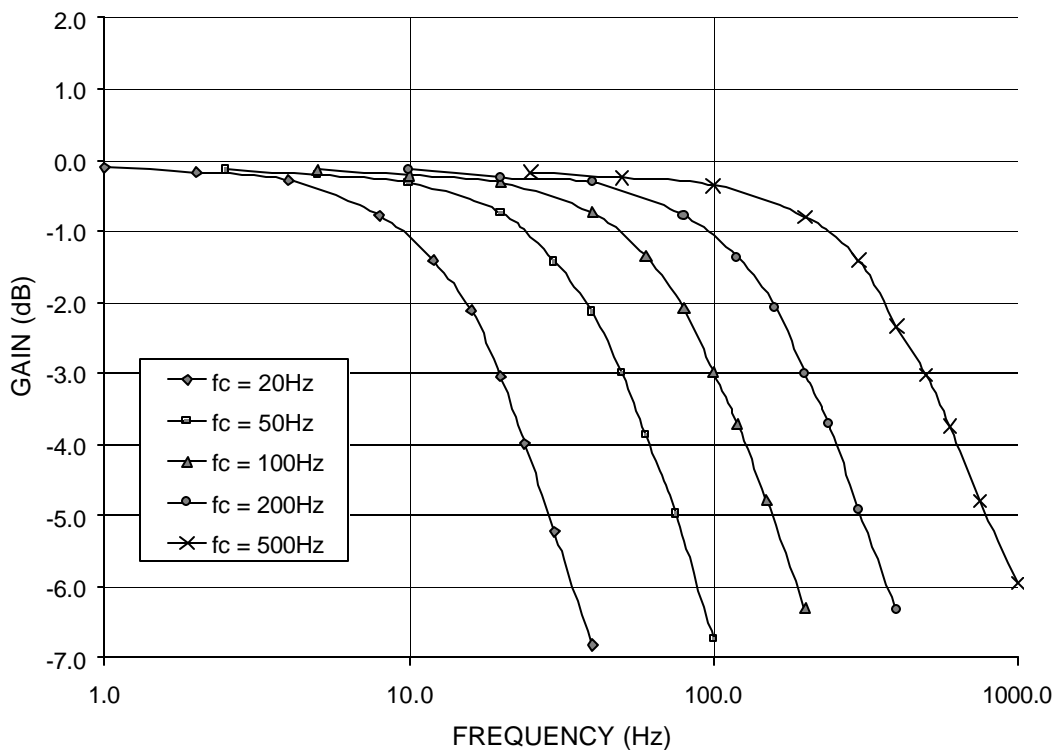


Fig. 12. Tuning of bulk CMOS filter circuit: Bode magnitude plots illustrating measured frequency response, with corner frequencies set (from left to right) to 20Hz, 50Hz, 100Hz, 200Hz, and 500Hz. Corresponding follower bias currents are approximately 13pA, 30pA, 59pA, 119pA, and 265pA, respectively. VPP is biased 0.5V below VDD. Input current is sinusoidal and ranges from 5nA to 15nA P-P.

When the mean input current is varied, no measurable effect is seen on the corner frequency of the filter over a decade range (mean currents from 5nA to 50nA). This confirms the independence of the filter time constant from filter state in this particular circuit configuration.

Total harmonic distortion with the corner and input frequencies set to 100Hz averages 1.6% in a sample of three die, a lower value than expected from simulation results. A sample plot from the spectrum analyzer is shown below in Fig. 13. For signals in the passband, measured distortion is on the order of 0.5%.

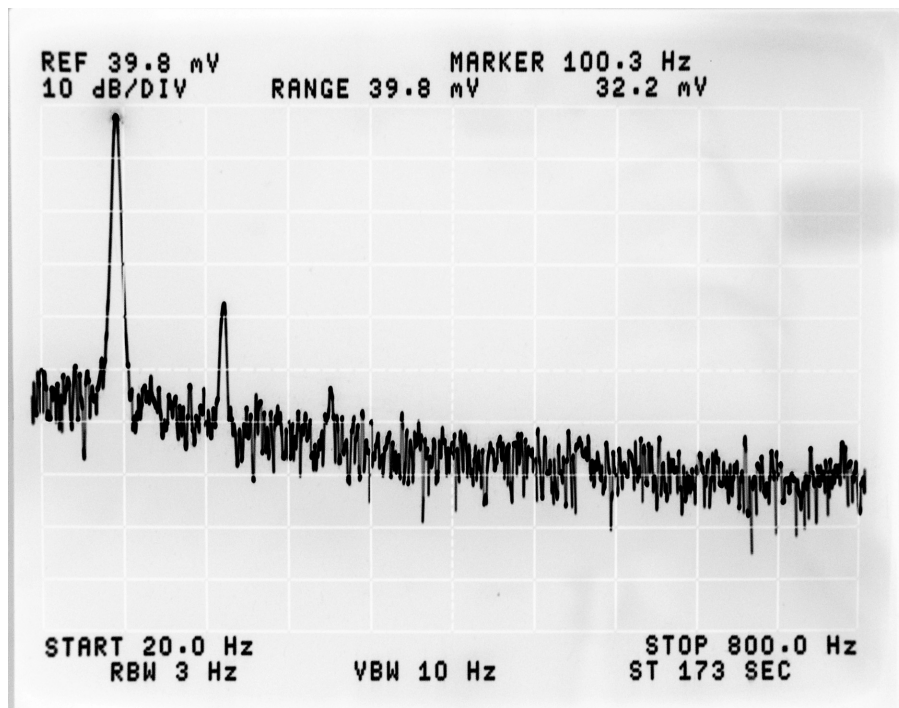


Fig. 13. Plot of spectrum of output signal of bulk CMOS filter circuit, with corner and excitation frequencies both set to 100Hz. Only the fundamental and first two harmonics are above the noise floor. Total harmonic distortion in this case is calculated to be 1.6%.

## VI. SUMMARY AND CONCLUSIONS

A simple methodology for implementation of current-mode, log-domain filters in CMOS technology has been presented. The basic unit circuit is a damped integrator. The transistors in the circuit that serve as nonlinear resistive elements are operated in weak inversion and in contrast with previous approaches may pass into the triode regime. The concept is particularly suited to implementation in silicon-on-insulator technology, because dielectric isolation of the transistors eliminates leakage currents, and because influence of the body effect on circuit

function does not result in large bias-related variations in the time constant. Very long time constants, on the order of 1s or more, are obtainable. Some simple elaborations of the basic circuit have been presented allowing the time constant to be controlled by a bias current. In addition, note has been made of potentially useful modes of nonlinear operation, including as a half-wave rectifier and lowpass filter, and by operation of the input and output devices in moderate to strong inversion, as a rapid-charge, slow-discharge damped nonlinear integrator.

Although a range of higher-order filter topologies based on the damped integrator unit are possible, it is anticipated that practical filter realizations in CMOS will be limited to relatively low-order, simple topologies due to device nonidealities and matching issues. Examination of significant nonidealities in bulk CMOS shows that junction leakage current is equivalent to a parasitic resistance to ground and does not affect the (pseudo)linearity of the circuit, while the body effect results in nonlinearity for large signals and in addition renders the time constant dependent on the mean filter state. This latter dependence can be eliminated with the use of a follower circuit of transistors of the same type as the filter itself, although the (pseudo)linearity of the circuit is still affected. The most significant nonidealities of bulk silicon are eliminated by implementation in silicon-on-insulator technology, although other sources of nonlinearity can arise due to differences between the effective body factors of the various devices in the circuit, and behavior of SOI devices under low bias conditions. In either technology, threshold voltage mismatches among input and output devices result in erroneous scaling of output currents, while among the nonlinear resistive elements, they influence the circuit time constant and cause (pseudo)voltage division errors in multiple-input circuits.

The basic damped integrator circuit, along with versions with electrically controllable time constants, were implemented in both bulk CMOS and an SOS CMOS process. Maximum time constants from hundreds of milliseconds to over one second were obtained, and tunability over many decades of frequency demonstrated in the electrically controllable circuits. These implementations demonstrate the viability of the basic concept, and as well illustrate some of the limitations that can be expected with such circuits.

This concept is regarded as particularly suitable for large-scale parallel circuits such as neuromorphic systems, in which precision and linearity may be of less importance than in traditional linear signal processing applications.

## ACKNOWLEDGMENTS

This work was supported by US Air Force Office of Scientific Research contract F49620-01-C-0030, and by US Air Force SBIR contract F08630-02-C-0013. The author thanks M. Sivilotti, S. al-Sarawi, A. Szeto, and an anonymous reviewer for helpful comments on the manuscript.

## REFERENCES

- [1] R.W. Adams, 'Filtering in the log domain.' Preprint 1470, 63<sup>rd</sup> AES Conference, New York, USA, 1979.
- [2] E. Seevinck, 'Companding current-mode integrator: a new circuit principle for continuous-time monolithic filters.' *Electronics Letters* vol. 26, no. 24, pp.2046-2047, 1990.
- [3] C. Tomazou, J. Ngarmnil, and T.S. Lande, 'Micropower log-domain filter for electronic cochlea.' *Electronics Letters* vol. 30, no. 22, pp.1839-1847, 1994.
- [4] M. Punzenberger and C. Enz, 'Low voltage companding current-mode integrators.' Proceedings, IEEE International Symposium on Circuits and Systems, Seattle, USA, pp. 2112-2115, 1995.
- [5] C.C. Enz, M. Punzenberger, and D. Python, 'Low-voltage log-domain signal processing in CMOS and BiCMOS.' Proceedings, IEEE International Symposium on Circuits and Systems, Hong Kong, pp. 489-492, 1997.
- [6] E. I. El-Masry and J. Wu, 'CMOS micropower universal log-domain biquad.' *IEEE Transactions on Circuits and Systems I*, vol.46, no. 3, pp. 389-392, 1999.
- [7] G.D. Duerden, G.W. Roberts, and M.J. Deen, 'The development of bipolar log-domain filters in a standard CMOS process.' Proceedings, IEEE International Symposium on Circuits and Systems, vol. I, pp. 145-148, Sydney, Australia, 2001.
- [8] B.A. Minch, 'Multiple-input translinear element log-domain filters.' *IEEE Transactions on Circuits and Systems II*, vol. 48, no. 1, pp. 29-36, 2001.
- [9] D. Python and C. Enz, 'Micropower Class-AB CMOS log domain filter for DECT applications.' *Journal of Solid-State Circuits* vol. 36, no. 7, pp. 1067-1075, 2001.
- [10] D.R. Frey, 'Log-domain filtering: an approach to current-mode filtering.' *IEE Proceedings G*, vol. 140, no. 6, pp. 406-416, 1993.
- [11] G.W. Roberts and V.W. Leung, 'Design of log-domain filters based on the operational simulation of LC ladders.' *IEEE Transactions on Circuits and Systems II*, vol. 43, no. 11, pp. 763-773, 1996.
- [12] D. Perry and G. Roberts, *Design and Analysis of Integrator-Based Log-Domain Filter Circuits*. Kluwer Academic Publishing, Boston, MA, 2000.
- [13] E. Vittoz and X. Arreguit, 'Linear networks based on transistors.' *Electronics Letters* vol. 29, no. 3, pp. 297-298, 1993.
- [14] Y. Tsvividis, 'Externally linear, time-invariant systems and their application to companding signal processors.' *IEEE Transactions on Circuits and Systems II*, vol. 44, no. 2, pp. 65-85, 1997.
- [15] J. Mulder, M.H.L. Kouwenhoven, W.A. Serdijn, A.C. van der Woerd, and A.H.M. van Roermund, 'Analysis of noise in translinear filters.' Proceedings, IEEE International Symposium on Circuits and Systems, Monterey, CA, USA, 1998.
- [16] A.E.J Ng and J.I Sewell, 'Direct noise analysis of log-domain filters.' Proceedings, IEEE International Symposium on Circuits and Systems, Scottsdale, AZ, USA, vol. III, pp. 309-312, 2002.
- [17] R. Sarpeshkar, T. Delbrück, and C. Mead, 'White noise in MOS transistors and resistors.' *IEEE Circuits and Devices*, vol. 9, no. 6, pp. 23-29, 1993.