

## **TANNER EDA BOOSTS IC DESIGN PRODUCTIVITY AND VERIFICATION CAPABILITIES WITH LATEST 13.0 RELEASE**

### **Full Verilog-A LRM 2.2 Compliance with T-Spice for Analog System-Level Simulation and Accurate 2D and 3D Hierarchical Parasitic Layout Extraction for Verification**

**Monrovia, CA – March 7th, 2008** – Tanner EDA, the leader in PC-based analog and mixed-signal IC design tools, today announced the release of HiPer PX and Verilog-A, two new powerful tools as part of Tanner Tools V13.0.

#### **Parasitic Extraction**

HiPer PX reduces design errors and shortens the design verification process by generating highly accurate RC models for interconnect parasitics that include higher-order moments and are guaranteed to be accurate up to a user-defined signal frequency. “As companies move further into deep sub-micron technologies, interconnect delays and second order coupling effects are becoming increasingly important in circuit simulations,” comments John Tanner, founder of Tanner EDA. “HiPer PX is an advanced parasitic extraction tool targeted for analog, mixed-signal and RF integrated circuits.”

HiPer PX is fully integrated within L-Edit, ensuring ease of use and minimal training time. It is available in two variants: HiPer PX2D extracts parasitics using a highly efficient boundary element estimation of parasitics, and HiPer PX3D which uses a highly accurate 3D finite-element method to extract vertical and lateral coupling capacitances. As a superset, HiPer PX3D includes all the capabilities of HiPer PX2D, and is capable of operating in either mode.

#### **System Level Analog Simulation**

T-Spice now incorporates a full Verilog-A implementation, enabling designers to easily and quickly write their own custom behavioral models for early system level simulations. Verilog-A enables the designer to do system level analog simulations much earlier in the design process. Verilog-A is featured as a cost option for the T-Spice simulator, and is included with Tanner’s HiPer Simulation and HiPer Silicon packages.

“By integrating Verilog-A capability, T-Spice customers can now very easily develop custom behavioral models in a standard, high-level language for a more predictable top-down design approach,” said Dr. Massimo Sivilotti, chief scientist, Tanner EDA. “For analog circuit designers, up until now, the lack of a behavioral language to functionally describe circuits means that designs are typically created and simulated from the bottom up, requiring costly redesign later when blocks are integrated and found to be incompatible.”

#### **Availability**

V13.0 will be released on March 31<sup>st</sup> and available for preview at the DATE Conference in Munich, Germany, March 10 ~ 14, 2008 – Tanner’s booth # F35. Demonstrations will also be presented at the DAC Conference in Anaheim, California, June 8 ~ 13, 2008 - Tanner’s booth # 1346. Tanner Tools are supported on Windows XP and Windows Vista

operating systems. For pricing and licensing information, contact Tanner EDA at [sales@tanner.com](mailto:sales@tanner.com) or call 1-877-325-2223 (inside U.S.) or 1-626-471-9701 (outside U.S.)

**About Tanner EDA**

Tanner EDA is a leading provider of easy-to-use, PC-based electronic design automation (EDA) software solutions for the design, layout and verification of analog and mixed-signal ICs and MEMS. For more information on Tanner EDA products, visit <http://www.tannereda.com>