

Enhanced design capabilities are found on HiPer Silicon v12.6

Monrovia, CA, May 23, 2007 – Tanner EDA, the leader in affordable, portable analog/mixed signals IC design tools, introduces HiPer Silicon™ v12.6, the new enhanced version of Tanner's complete suite of schematic capture, analog SPICE simulation, physical layout and foundry compatible DRC.

The new S-Edit™ Schematic Capture includes new connection hotspot on pins and ports making wiring and current probing quicker and easier. Multiple pages schematics allow straightforward creation and organization of large complex schematics. Rendering and editing performance has been greatly improved, especially on schematics with large number of symbols. SPICE export now features faster export and simpler SPICE output specifications. Probing of small signal parameters can now be done for devices modeled as subcircuits.

T-Spice™ Analog SPICE simulation has been enhanced with multi-threaded support for faster runtimes, with added support for the RPI Amorphous-Si and Poly-Si TFT models. All Philips models (MOS9, MOS11, MEXTRAM, PSP and others) have been updated to the latest v2.4 release. Transient analysis performance improvements for faster runtimes and shorter design cycles are also included. Polynomial controlled source devices have been extended to 6th order and enhanced with new options for limiting and modifying the output currents of voltages.

L-Edit™ Physical layout can now stretch instances and arrays automatically adjusting their repeat counts. T-Cells can be configured to be stretchable which modifies the stretch parameters by the stretch amount and then regenerates the T-Cell. Enhancements have been added for automatic guard ring generation by using objects, wires, polygons, or boxes to designate the path of the ring.

HiPer Verify™ is now able to perform antenna rules checks including NET AREA RATIO, NET AREA, NET AREA RATIO PRINT, and incremental connectivity extraction (DRC INCREMENTAL CONNECT & DISCONNECT). Significant performance improvements have been made, in some cases up to 10x faster than previous versions especially in designs dominated by large arrays. Calibre® compatibility has been enhanced with support for opposite extended measurement metric, CMACR/DMACRO, ORNET, and SHIFT.

Tanner Tools are Windows® based, supporting Windows XP and Windows® Vista™. The beta version of HiPer Silicon v12.6 will be available for preview at the DAC Conference, June 4 ~ 7, 2007 in San Diego, and will be ready to ship by the end of June. Contact Tanner EDA at sales@tanner.com or call 1-877-325-2223 (inside U.S.) or 1-626-471-9701 (outside the U.S.) for pricing and licensing information.

About Tanner EDA

Tanner EDA is a leading provider of easy-to-use, PC-based electronic design automation (EDA) software solutions for the design, layout and verification of analog/mixed signal ICs and MEMS. Its solutions help speed designs from concept to silicon and are used by thousands of companies to develop devices cost-effectively in next-generation wireless, consumer electronics, imaging, power management, biomedical, automotive and RF market segments. Founded in 1988, Tanner EDA is a division of privately held Tanner Research, Inc.

For more information about Tanner EDA visit: <http://www.tannereda.com>

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