

COMPANY NEWS



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CHIP DESIGNERS CAN SAVE VALUABLE TIME WITH NEW TANNER TOOLS 12.2 FOR ANALOG AND MIXED-SIGNAL DESIGN

PERFORMANCE UPGRADE, NEW FEATURES SPEED DESIGN-TO-CHIP PROCESS AND MAKE TOOLS EASIER TO USE

Monrovia, Calif., Jan. 8, 2007 – Tanner EDA, which provides cost-effective, easy-to-use, Windows®-based tools for analog and mixed-signal circuit design, today announced the immediate availability of Tanner Tools 12.2, the latest version of its integrated tool suite for schematic capture, simulation, physical layout and verification.

“Tanner Tools continues to add value and efficiency for analog and mixed-signal designers. Our latest performance enhancements and new features provide for a more tightly integrated and highly functional tools set that continues to evolve to meet the needs of our customers,” noted Dr. Massimo Sivilotti, chief scientist, Tanner EDA.

Tanner Tools 12.2 New Features and Speed Enhancements

Tanner Tools 12.2 includes new features and updates for S-Edit, T-Spice, L-Edit and HiPer Verify. S-Edit provides schematic capture, which offers netlist input and output and tight integration with analog simulation, as well as the ability to perform Schematic Driven Layout. The latest S-Edit enhancements include:

- Faster EDIF import and export, SPICE export and design load and save
- Ability to import and export Cadence-compatible EDIF files
- Callback functions for properties
- Print preview feature and optimized black-and-white printing performance

T-Spice circuit simulation, which currently includes HSPICE/PSpice compatibility and support for the latest industry models, now features faster performance as well as improved operating point convergence using pseudo-transient analysis and new homotopies.

L-Edit, Tanner’s physical layout editor, now offers:

- Layer palette that displays layer names and icons
- Integrated layer manager that allows users to define layers as locked or selectable
- Capability to automatically convert layouts to T-cell code

- DevGen feature, which creates T-cells for common devices (transistors, resistors, capacitors) with L-Edit Schematic Driven Layout (SDL)
- Expanded support for small feature sizes that are more common in new designs
- Ability to undo auto-placement of vias, contacts and guard rings

HiPer Verify, which offers foundry-compatible, hierarchical design rule checking, now saves valuable design time by running checks from 2 to 10 times faster.

New Program Smooths Transition to Tanner

Tanner also announced that it will extend its SmoothSwitch offer to include the new Tanner Tools 12.2. SmoothSwitch offers significant discounts and a support program to help users of ICED tools make the transition to Tanner EDA. For more information on the SmoothSwitch offer, go to www.tannereda.com/smoothswitch.

Availability and Pricing

Tanner Tools 12.2 is available now. Pricing varies depending on geography and licensing. For pricing and licensing information, contact Tanner EDA at sales@tanner.com or call 1-877-325-2223 (inside U.S.) or 1-626-471-9701 (outside U.S.).

About Tanner EDA

Tanner EDA is a leading provider of easy-to-use, PC-based electronic design automation (EDA) software solutions for the design, layout and verification of analog/mixed signal ICs and MEMS. Its solutions help speed designs from concept to silicon and are used by thousands of companies to develop devices cost-effectively in next-generation wireless, consumer electronics, imaging, power management, biomedical, automotive and RF market segments. Founded in 1988, Tanner EDA is a division of privately held Tanner Research, Inc.